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Software Defined Receiver

Digital signalprocessing in an FPGA

Agenda

- Introduction
- Assignment
- Ideal solution
- Practical solution
- Implementation

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Introduction

- Who am I?
  - Antoine Hermans, CTO
- Who is Adeas?
  - Independent Design House located in Eindhoven since 2005.
  - Developers of customer specific electronic products, embedded systems and IP.
  - Adeas specializes in FPGA and SoC based designs on advanced digital and mixed signal boards
  - Design Partner of Intel FPGA (formerly Altera) and Xilinx

intel FPGA Design Solutions Network Platinum

XILINX ALLIANCE PROGRAM CERTIFIED MEMBER — BASE

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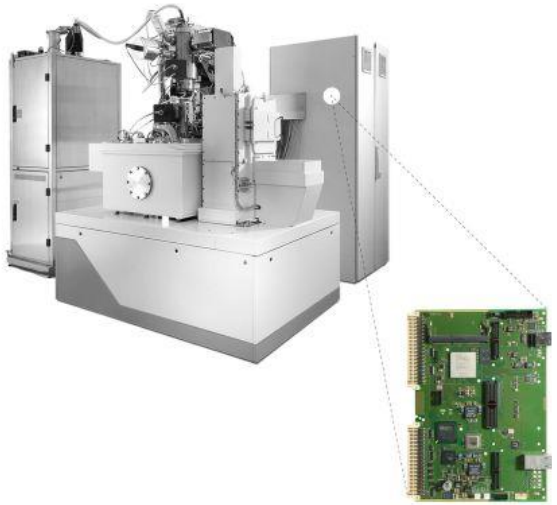
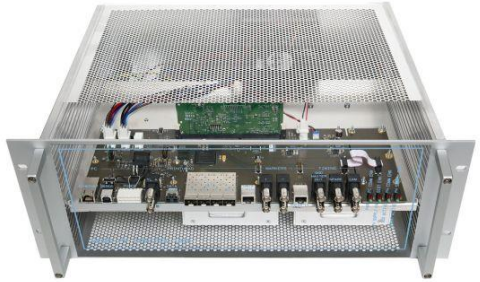
Introduction

- Broadcast
- Video & Imaging
- High Tech Industrial
- Test & Measurement





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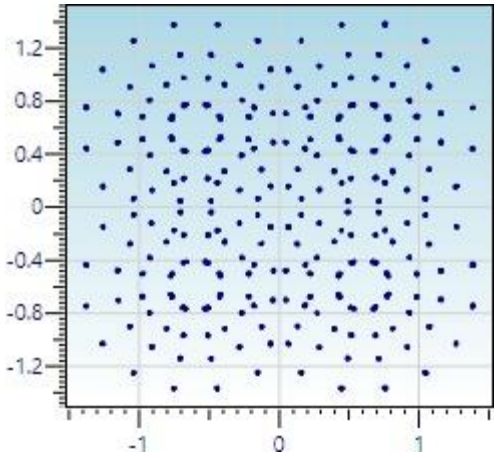
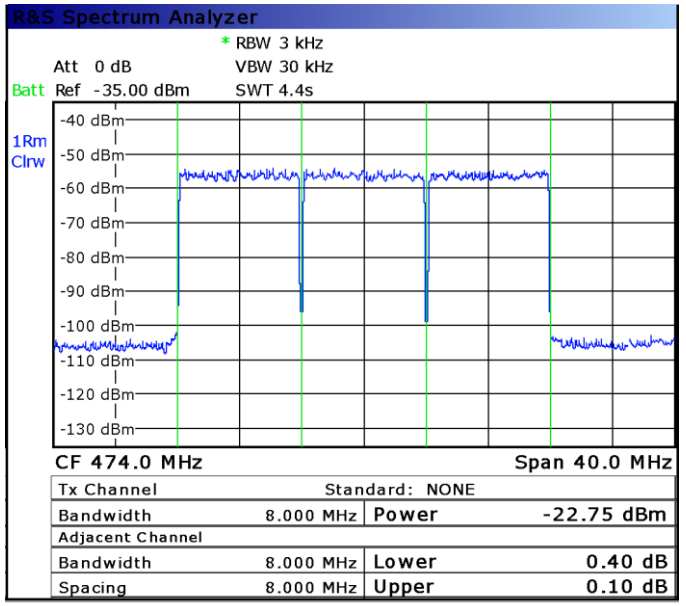
Assignment

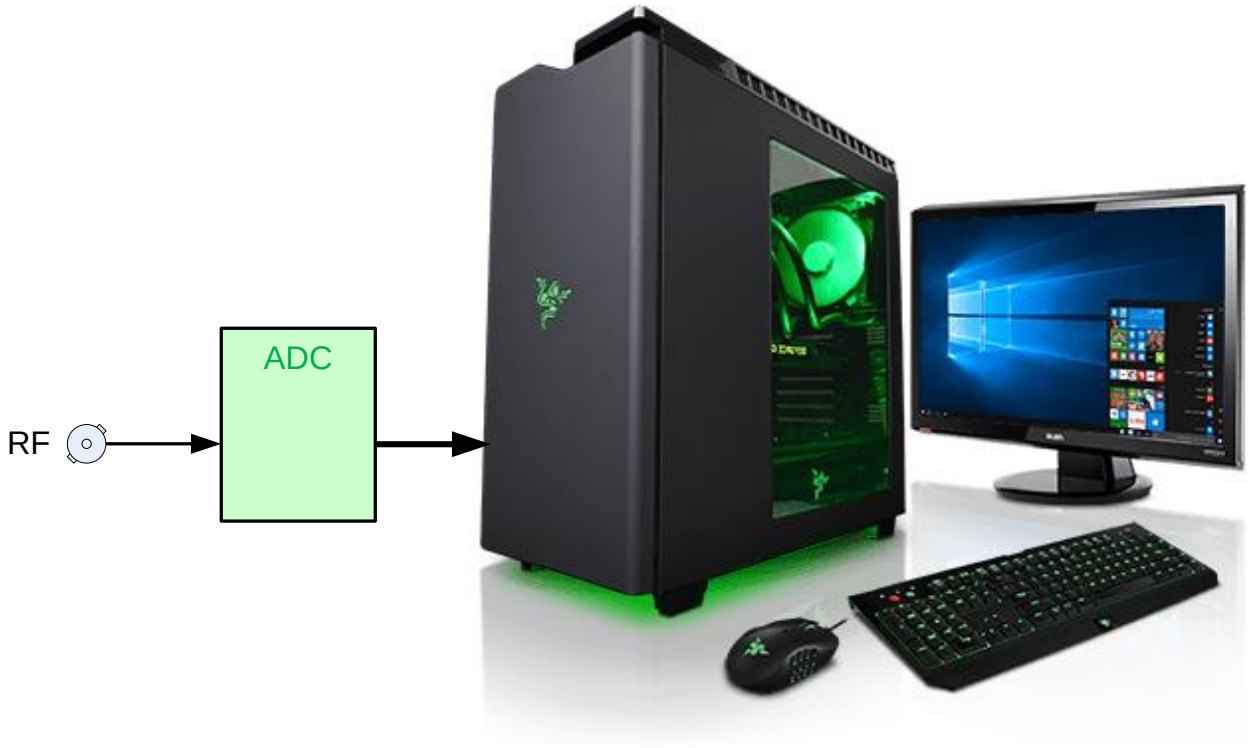
- Design a front-end for a software defined receiver / RF analyser
  - For (professional) audio and video applications
  - Able to measure RF Characteristics like channel power and MER
  - As accurate as possible
  - Versatile (different modulation standards)
  - Prepared for future standards
  - Cost effective





Ideal solution w.r.t. quality and flexibility

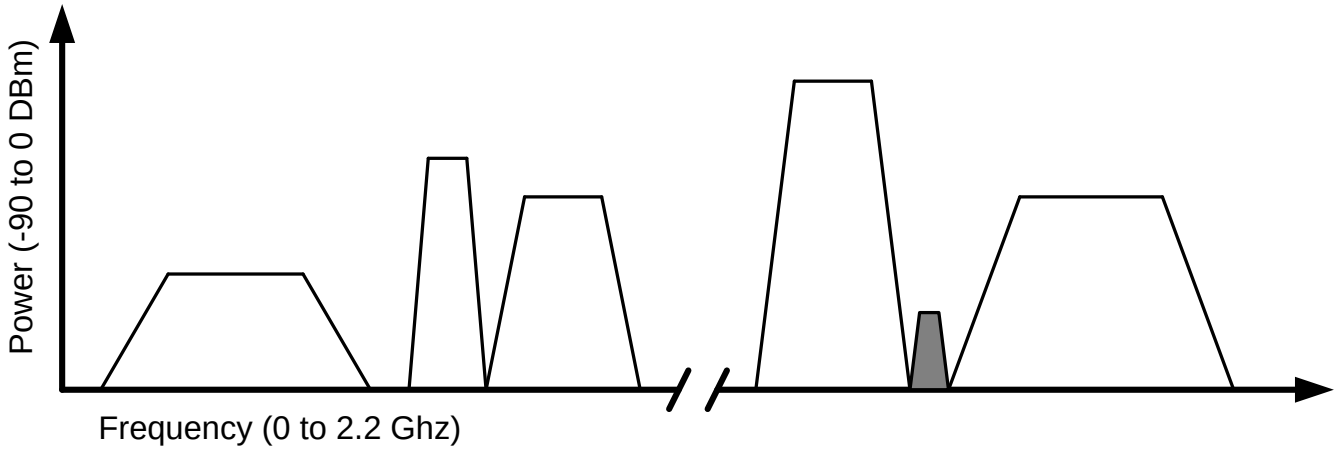
- No analog processing -> All digital processing
- Digital processing can be as accurate as you want
- All processing done on a standard PC



Ideal solution not possible / practical

- Large amount of computations per second in SW -> not practical
  - High sample rate needed to cover 2.2 GHz analog freq. spectrum

- High amount of effective number of bits in ADC -> does not exist yet
  - Dynamic range / sensitivity
  - Difference in channel power of (adjacent) channels
  - Loss of effective number of bits due to filtering



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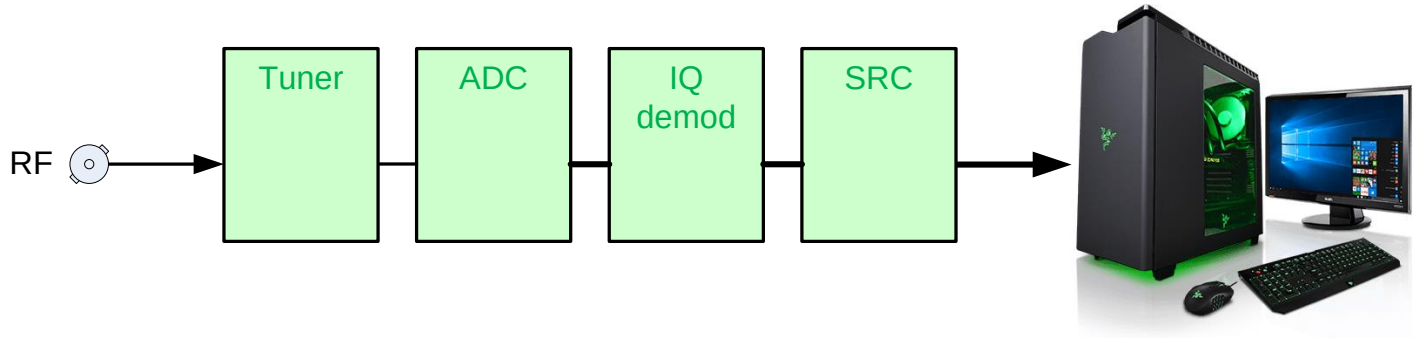
Practical solution



- Use ‘analog’ tuner wit gain stages and filtering
  - Lower sample rate of ADC
  - less ENOB needed
- Use FPGA to reduce SW processing power needed
  - IQ demodulation in FPGA
  - Additional filtering in FPGA
  - Sample rate conversion in FPGA
  - Characteristics (channel power) measurement in FPGA

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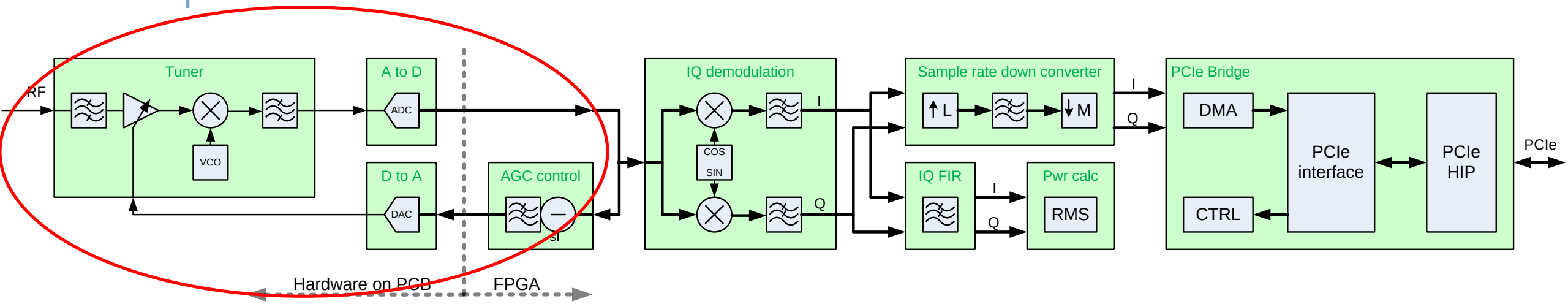
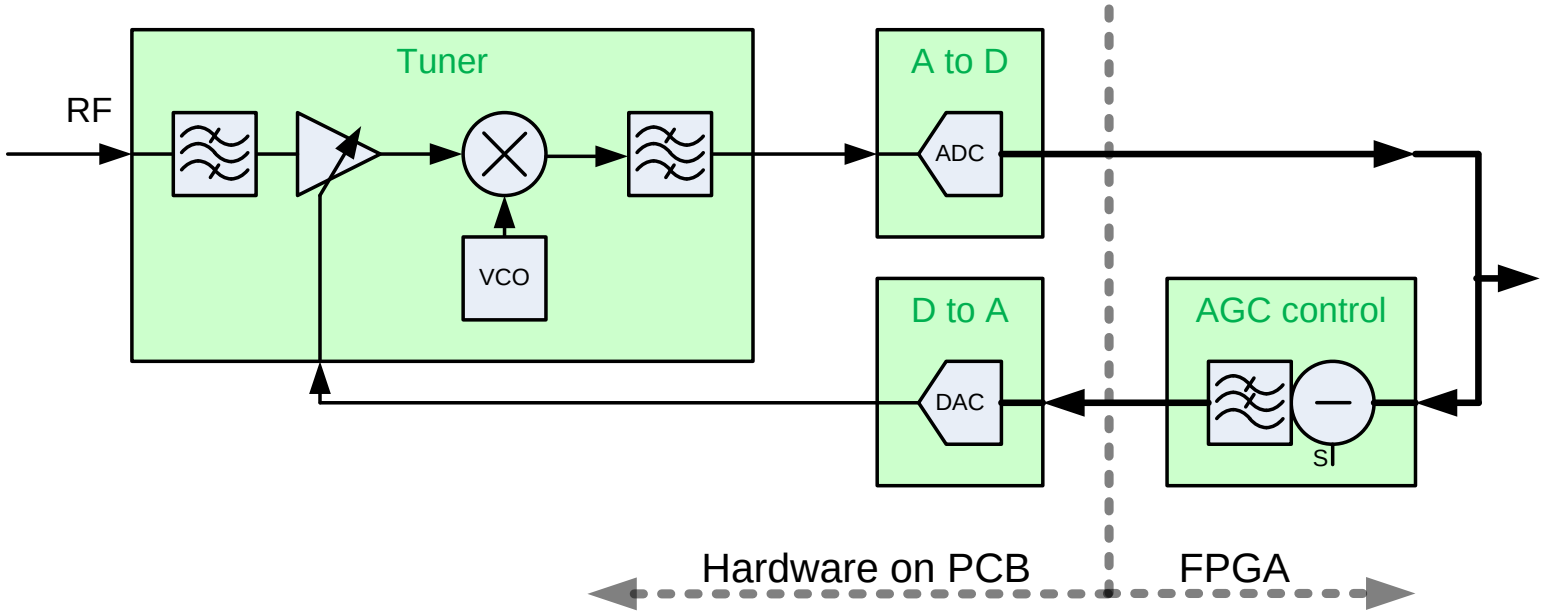
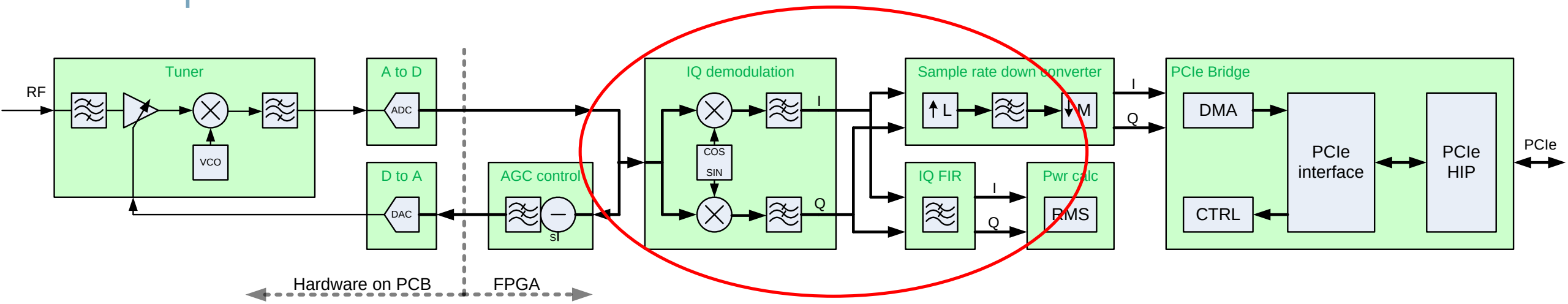
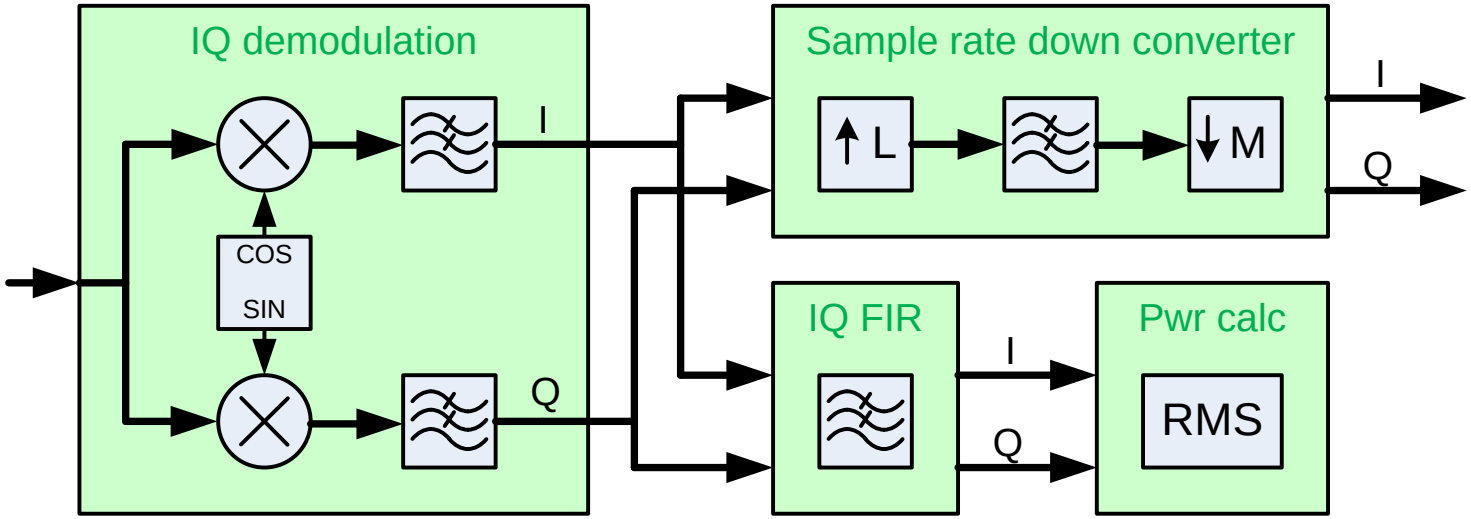
Implementation





Implementation





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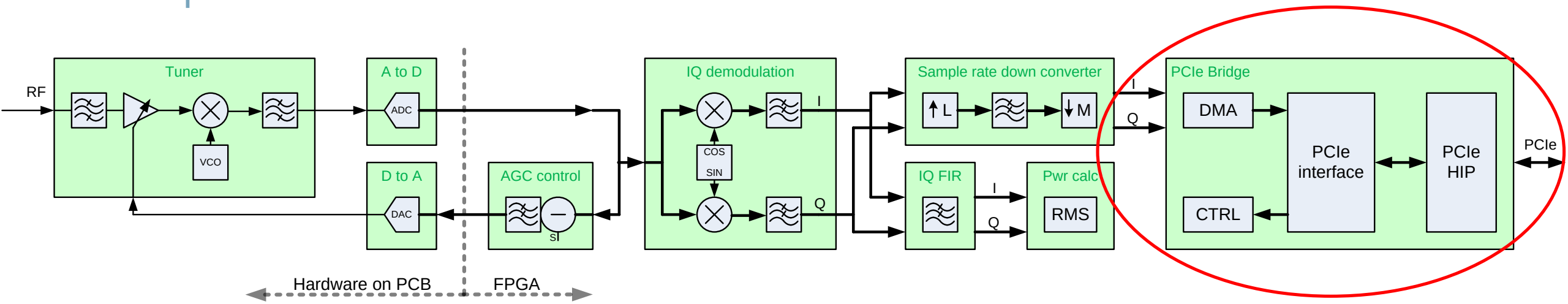

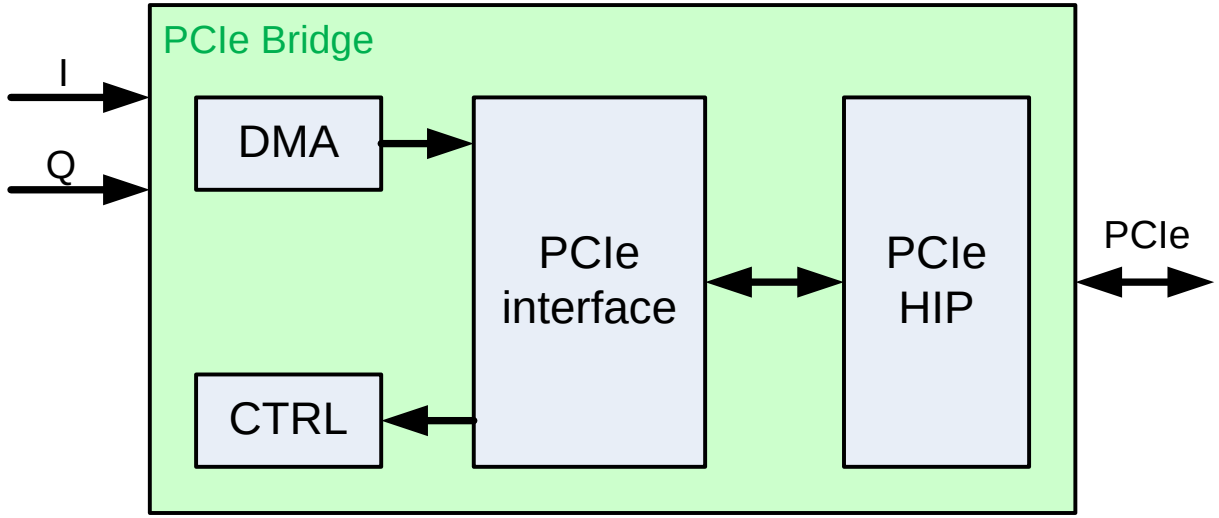

SW defined / fixed implementation

- SW defined
  - Programmable tuner frequency
  - Programmable filter sections in tuner
  - Programmable ADC sample rate
  - Programmable IQ demodulation frequency
  - Programmable AGC thresholds / characteristics
  - Programmable filter coefficients
  - Programmable down conversion factor
- Fixed
  - Choice of the tuner used
  - FPGA functions specific for the application
  - Design choices like internal data bus width and numeric precision

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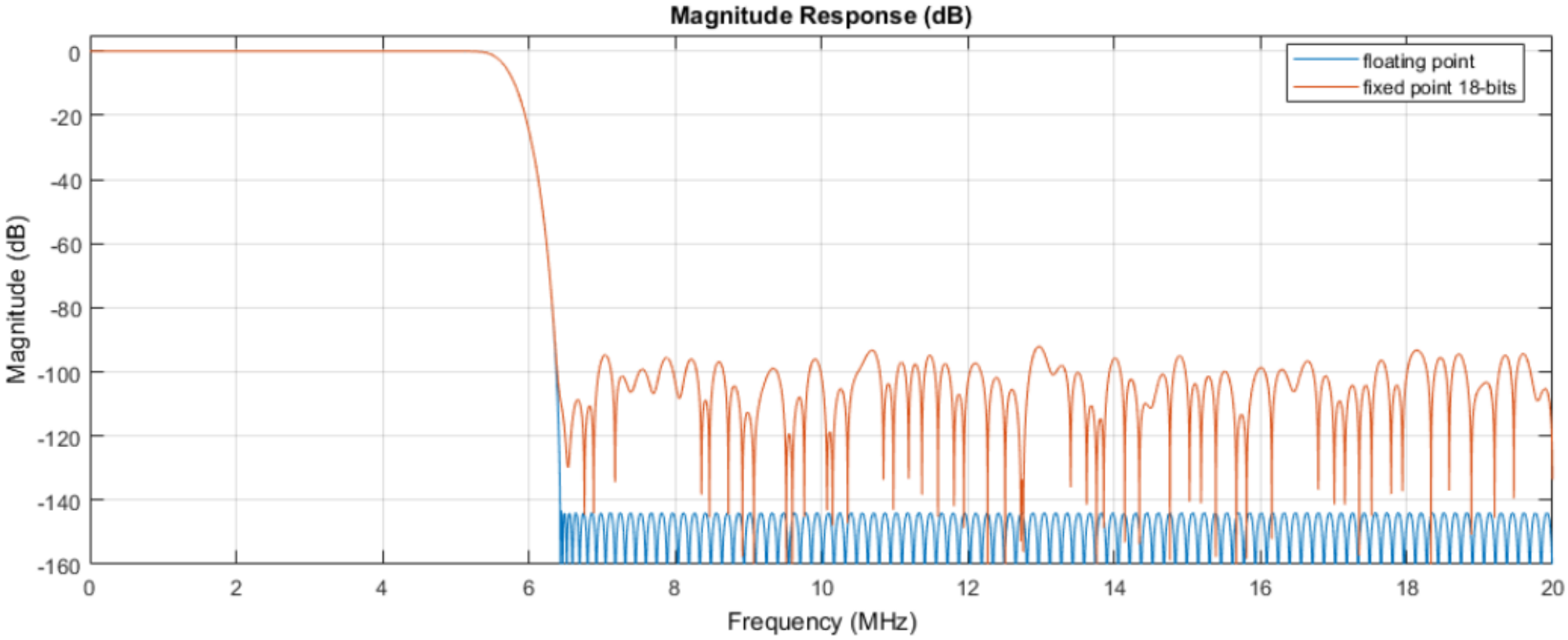
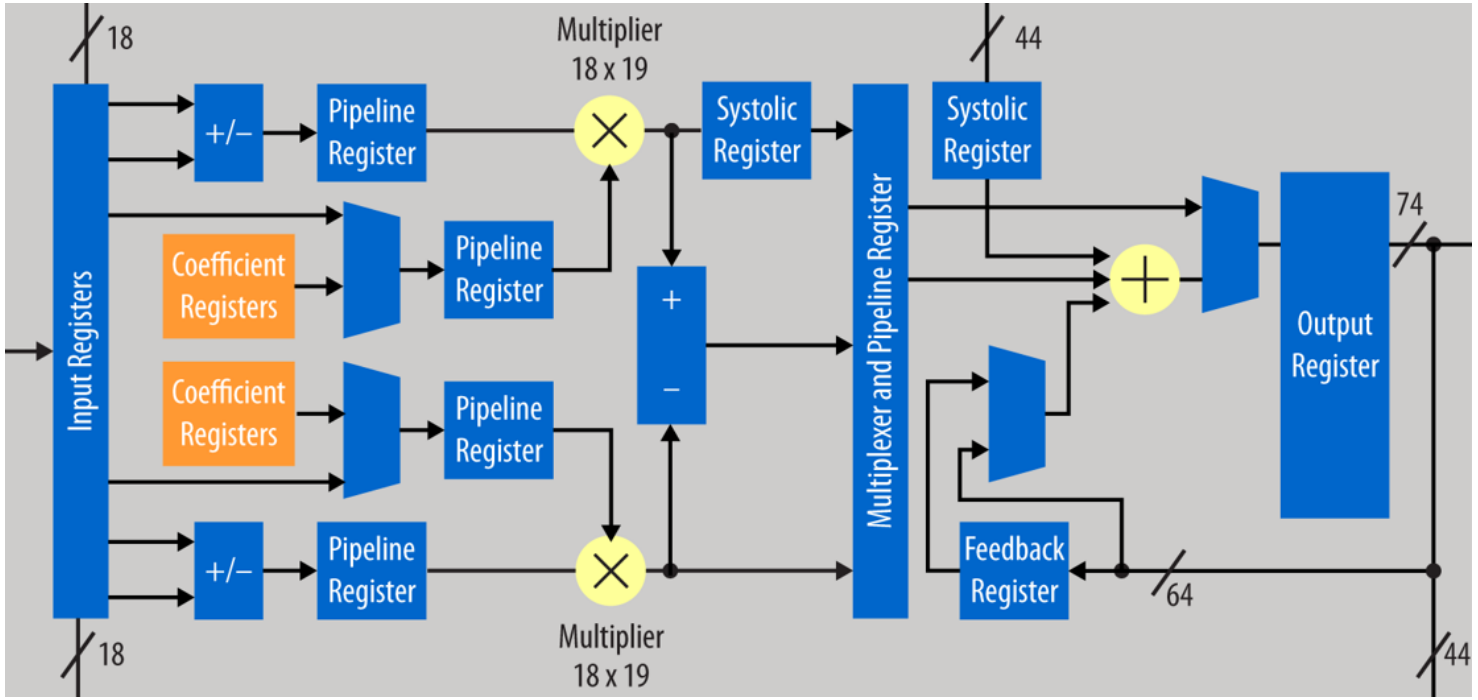
Precision

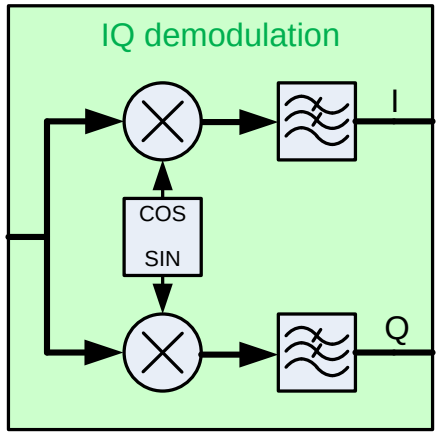
- Bus width: 18 bit signed
- Filter coefficients: 18 bit signed
- Number of taps in FIR filter: e.g. 256 taps



Resources / optimization

- Amount of bits, mapped to DSP resources of FPGA
- DSP resources scales with amount of taps, but can be optimized
- Clock frequency. Headroom can be used to multiplex in time





Questions?