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Ultra HD using Low Cost FPGA's

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&
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Introduction

Who are we?

- Frans Kennis, Senior Designer/Architect
- Antoine Hermans, CTO

Who is Adeas?

- Independent Design House located in Eindhoven.
- Development of customer specific electronic products, modules and embedded systems from feasibility to product delivery.
- We serve customers active in multimedia, broadcast & communication, printing & imaging, high tech machinery, semiconductor, medical, infrastructure and defense industries.

Specialised in FPGA & SoC design.

- Extensive experience, advanced tooling, optimised process & environment, large team of designers
- Design Partner of both Altera and Xilinx

Agenda

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- Introduction to UltraHD Video
- 4K-SDI Product Specifications
- Architecture Challenges using Low Cost FPGA's
- Results

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Introduction to UltraHD Video

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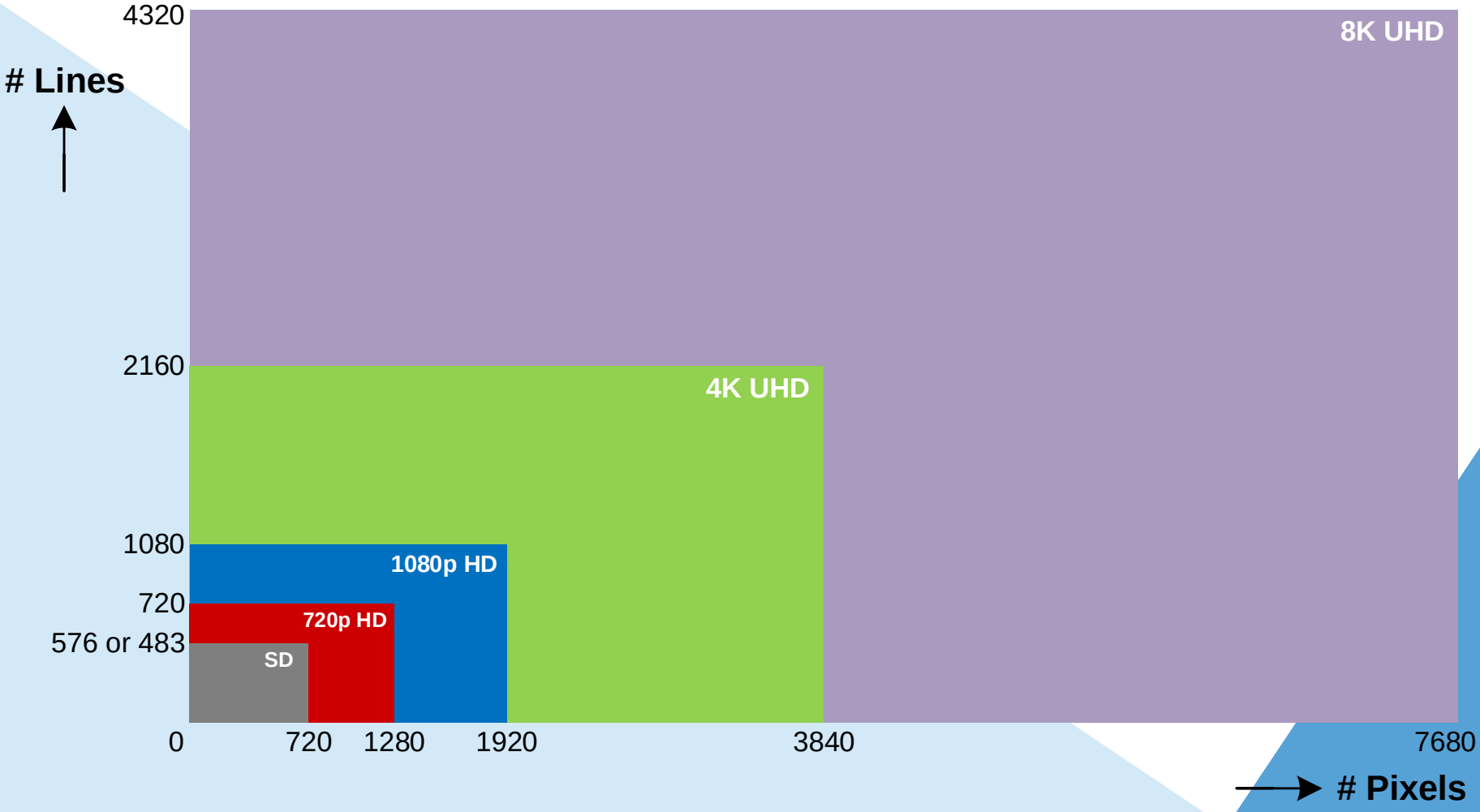

Introduction to UltraHD Video

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Uncompressed SDI Bitrates (Gbit/s)		HD	4K-UHD	8K-UHD
Frame Rate > 60-120 fps	12-bit 4:4:4	12	48	192
	10-bit 4:2:2	6	24	96
Frame Rate 30-60 fps	12-bit 4:4:4	6	24	96
	10-bit 4:2:2	3	12	48
Frame Rate < 30 fps	12-bit 4:4:4	3	12	48
	10-bit 4:2:2	1.5	6	24

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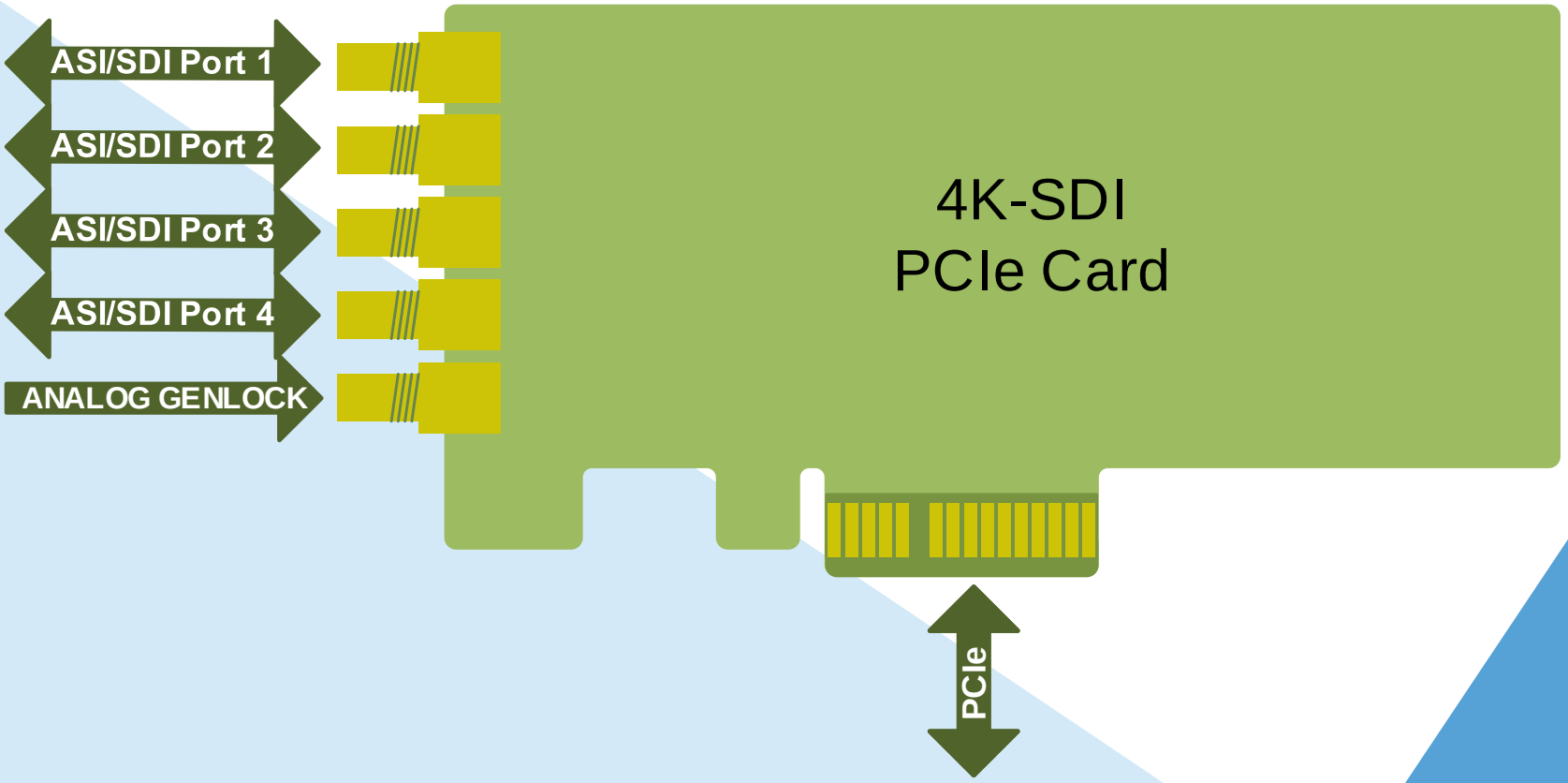
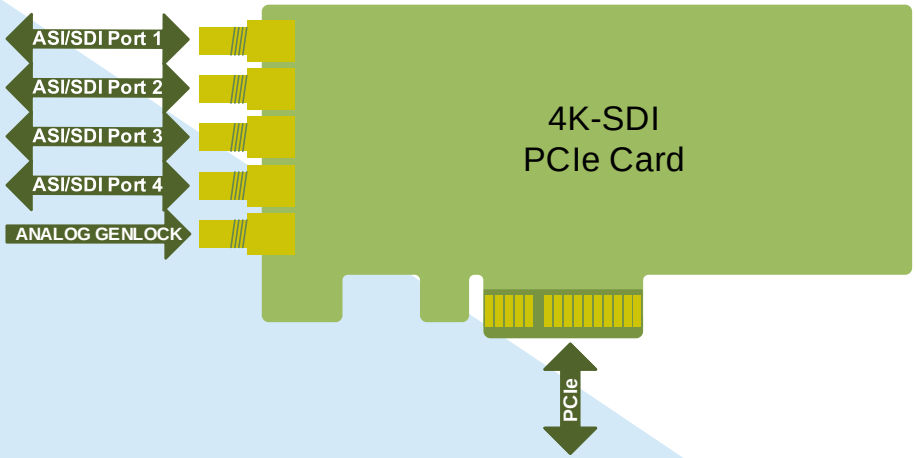
Product Specifications



Product Specifications



- PCIe card; Low profile
- Four I/O ports selectable between Input and Output
- Analog and Digital GenLock

- Power consumption < 25 Watt
- Support of ASI and SD/HD/3G/12G(4K) –SDI
  - 4K-SDI transferred via 4 x 3G-SDI ports
  - Multiple (>20) SDI standard support
  - SDI format can be selected for each channel separately

Product Specifications

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Architecture Challenges:

- "Easy" SDI frames processing by software
- Robustness for non-realtime operating systems
  - Enough margin in PCI Express and memory bandwidth
- Low cost price

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Architecture Challenges (HW)

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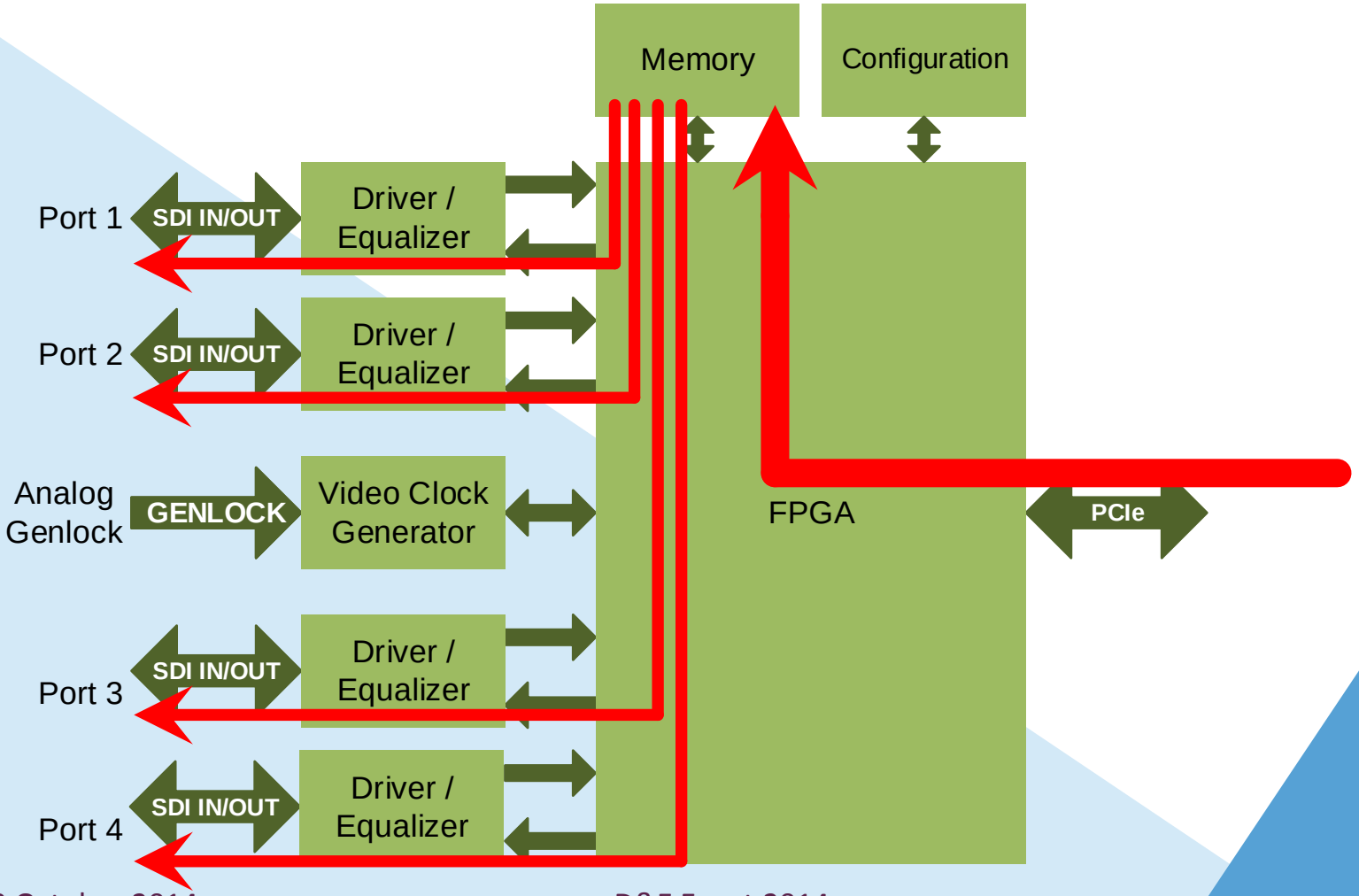
4K-SDI PCIe Card : Basic Architecture



Architecture Challenges (SW)

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“Easy” SDI frames processing by software:

- Align pixels op 16-bits boundaries
  - Increase of PCIe bandwidth
- Align lines on user defined boundaries
  - E.g. Every line uses 64 kbyte memory
  - Increase of PCIe bandwidth
- Implement 1/4 or 1/16 Scalers in FW
  - Reduction of PCIe bandwidth
- Implement Direct DMA functionality

Architecture Challenges (HW)

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Needed PCI Express bandwidth:

- PCIe needed bandwidth:

Pixel Width	PCIe Bandwidth
10-bits	12 Gbit/s
16-bits	19.2 Gbit/s

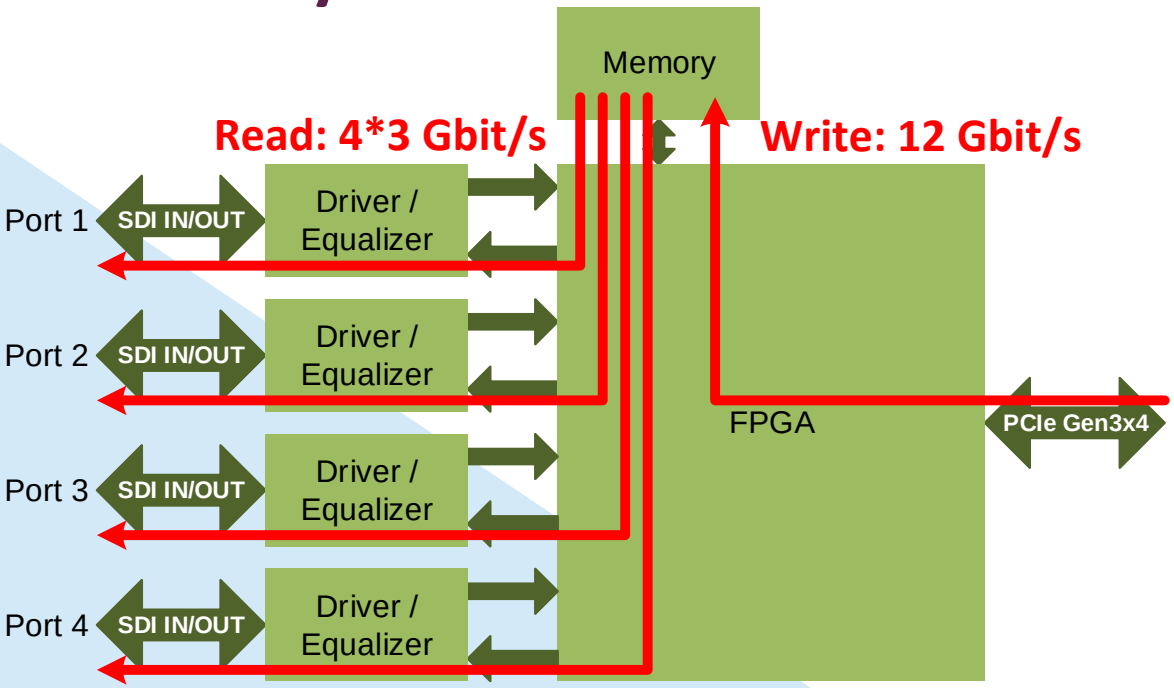
- 25 % headroom wanted on PCIe interface:

  19.2 Gbit/s + 25 % = 24 Gbit/s

- PCIe Gen3x4 available bandwidth : 31.5 Gbit/s
  - ➢ Needed efficiency > 76% !

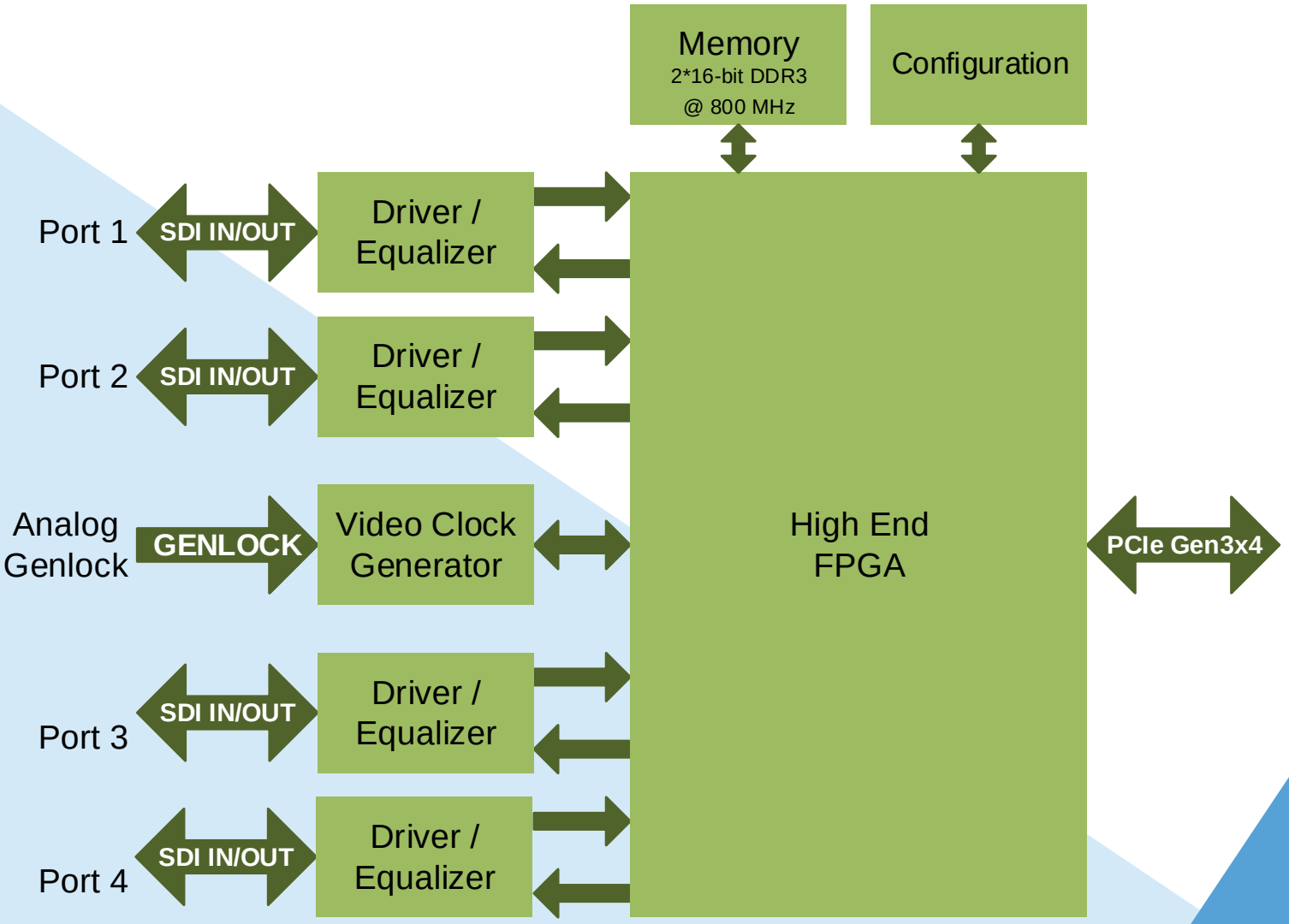
Architecture Challenges (HW)

Needed memory bandwidth:



- Needed memory bandwidth:
  - Write 12 Gbit/s + Read 12 Gbit/s + 25 % headroom = 30 Gbit/s
- Available mem bandwidth (2*16-bit DDR3 devices@800MHz):
  - 800 MHz * 2 * 32 bits = 51.2 Gbit/s (needed efficiency > 59 %)

Architecture Challenges (HW)



Architecture Challenges (HW)

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Challenges using low cost FPGA:

- PCIe GEN3x4 not available
- 800 MHz memory controller not available
  - Use of 4 * 16-bit DDR3 devices @ 400 MHz → # I/O pins ??
- Not enough clock resources
  - All ports can operate at different SDI formats. This needs a lot of different clocks

Architecture Challenges (HW)

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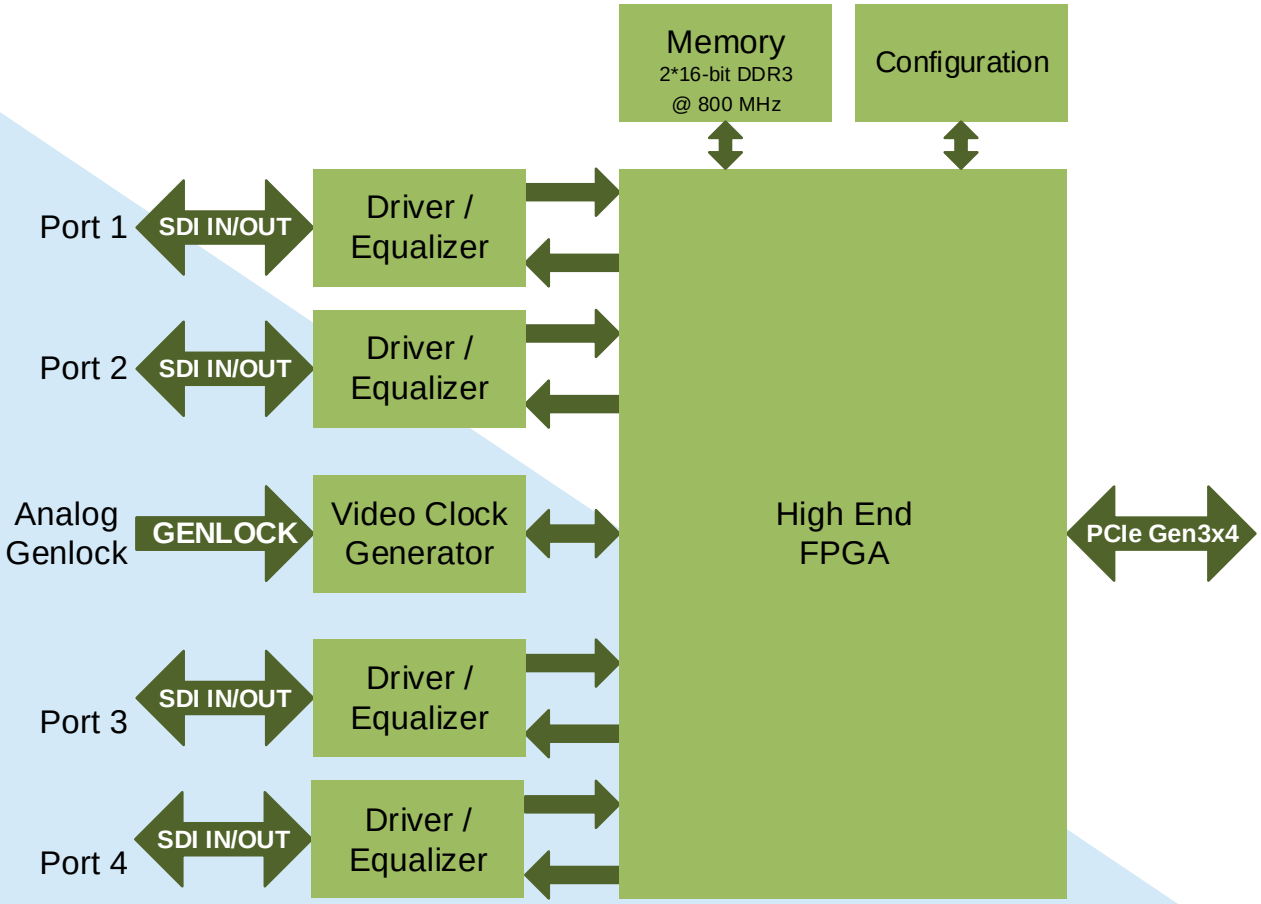
PCIe GEN3x4 with low cost FPGA's

- PCIe support in Altera FPGA's:

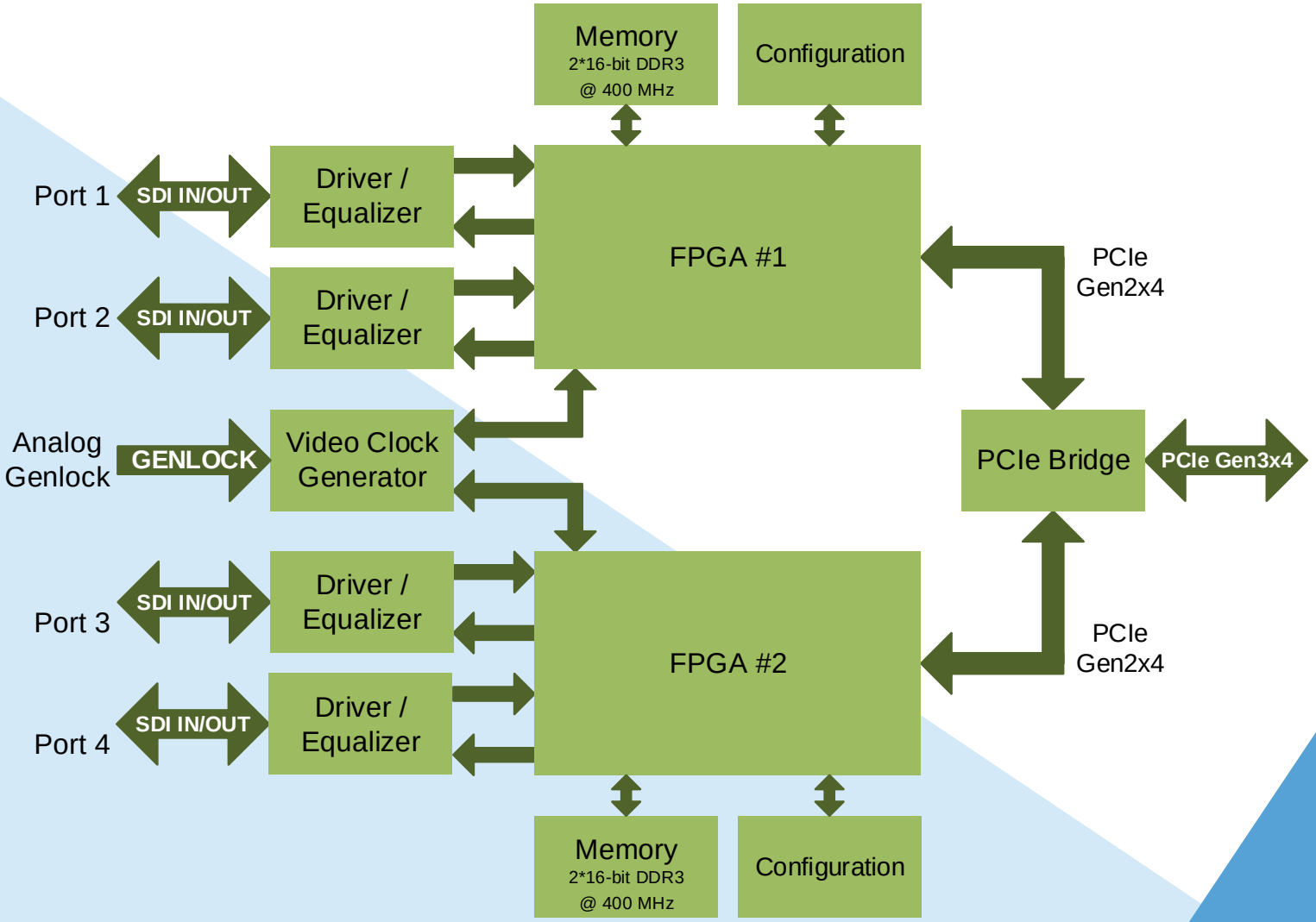
FPGA	Cost Price	PCIe Generation	Pcie #Lanes
CycloneIV-GX	Low	GEN1	x1, x2, x4
CycloneV	**Low**	**GEN2**	**x4**
Arria II	Medium	GEN1 GEN2	x1, x2, x4, x8 x1, x2, x4
ArriaV-GX/GT	Medium	GEN1 GEN2	x1, x2, x4, x8 x1, x2, x4
StratixV/ArriaV-GZ	**High**	**GEN3**	**x4**

- Use 2 Cyclone V FPGA's with PCIe bridge

Architecture Challenges (HW)



Architecture Challenges (HW)



Architecture Challenges (FW)

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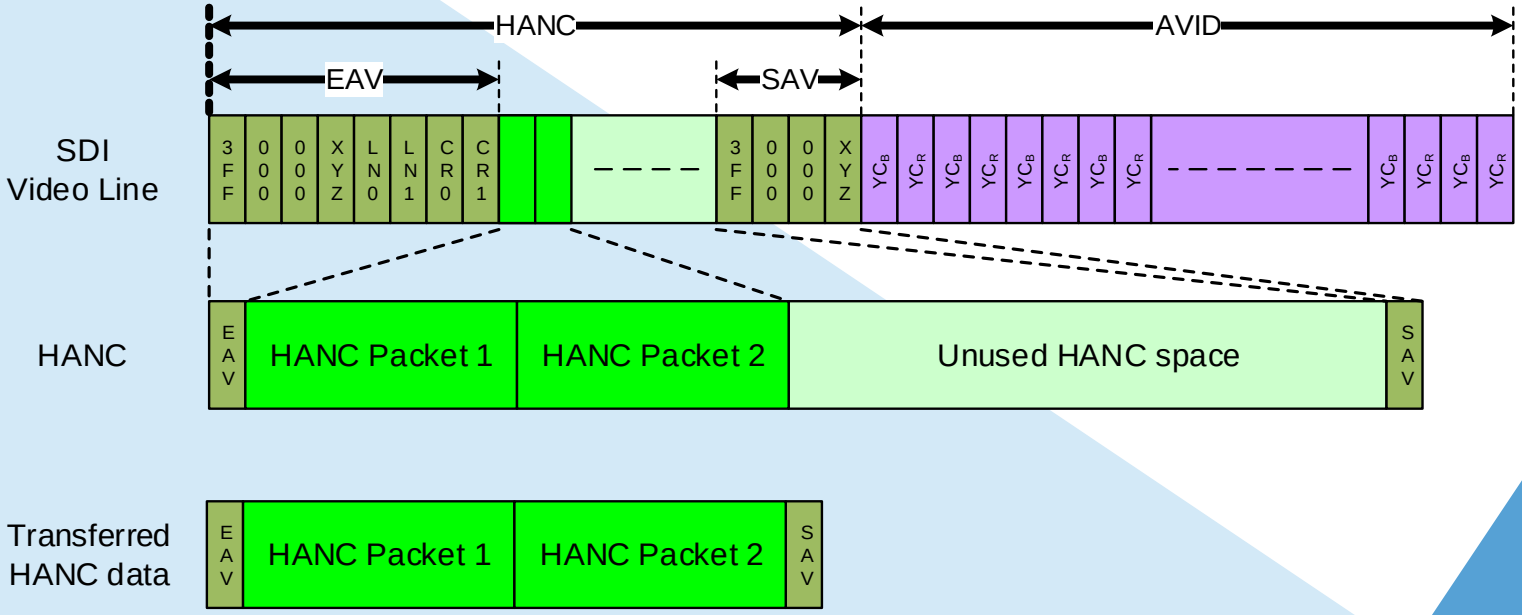
Firmware challenges using low cost FPGA's:

- Achieve required bandwidth on PCIe interface
- Needed system clock frequency too high

Architecture Challenges (FW)

Achieve required bandwidth on PCIe interface (12 Gbit/s):

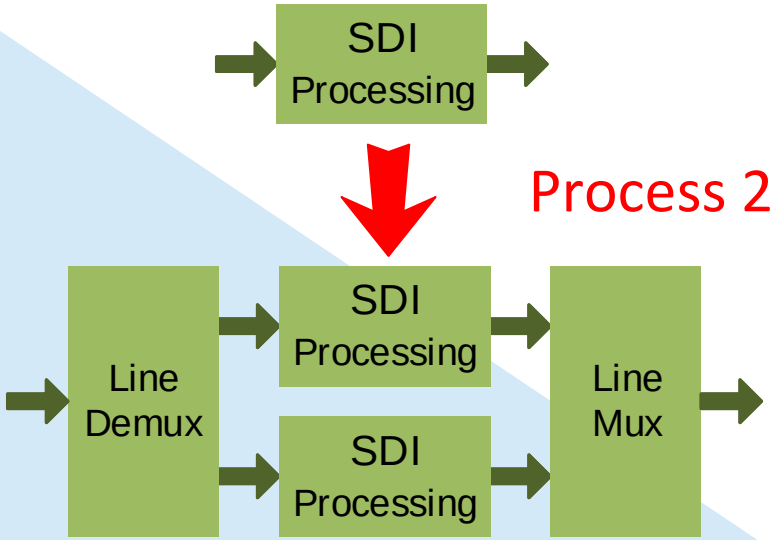
- Use multiple DMA controllers
- Use prefetching in the DMA controllers
- Don't transfer unused HANC/VANC data



Architecture Challenges (FW)

System clock frequency too high for low cost FPGA:

- 3G-SDI video clock : 148.5MHz @ 2 * 10-bits pixels
- Needed system clock frequency: 148.5 MHz + 25 % spare = 185 MHz
- Maximum clock frequency Cyclone V ≈ 150 – 160 MHz



- Selected system clock 135 MHz (→270 MHz @ 20-bits)

Architecture Challenges (SW)

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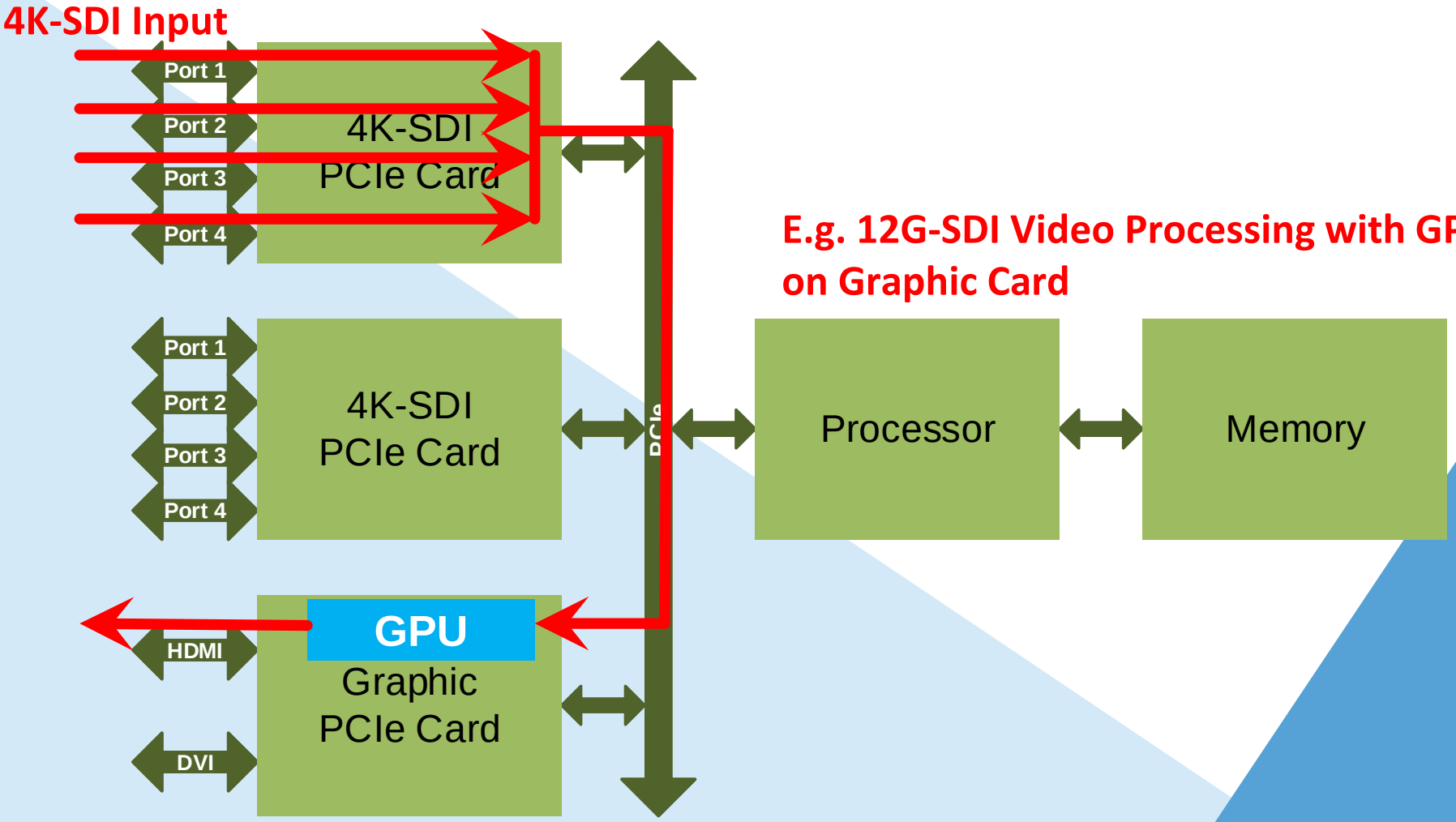
Application with Direct DMA functionality



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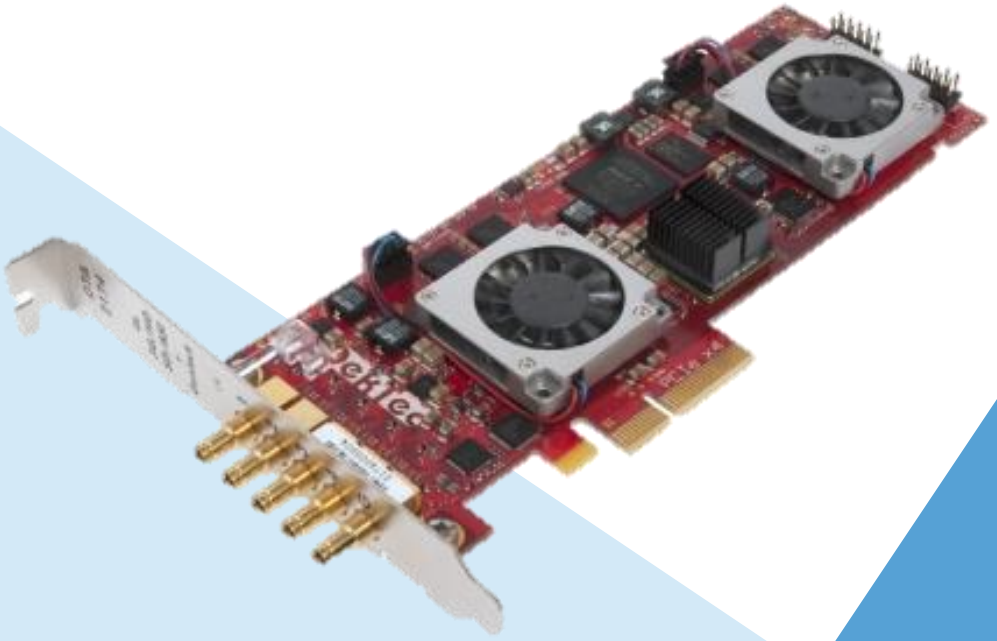
Results

- 4K-SDI PCIe card with 2 Low Cost CycloneV FPGA's
- Power consumption ≈ 19 Watt
- All requirement specifications are met



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Questions?

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Thank you for your attention!